UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/826,693	04/04/2001	Mario Nemirovsky	P3819	4332

24739	7590	10/04/2004

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EXAMINER
BRAGDON, REGINALD GLENWOOD

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 10/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>*13 April 2004 and 27 July 2004*</u>.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

     4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

     a)☐ All b)☐ Some * c)☐ None of:

         1.☐ Certified copies of the priority documents have been received.

         2.☐ Certified copies of the priority documents have been received in Application No. _____.

         3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

     * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
     Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
     Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1.   A request for continued examination under 37 CFR 1.114, including the fee set forth in

37 CFR 1.17(e), was filed in this application after final rejection. Since this application is

eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e)

has been timely paid, the finality of the previous Office action has been withdrawn pursuant to

37 CFR 1.114. Applicant's submission filed on 27 July 2004 has been entered.

Information Disclosure Statement

2.   The Information Disclosure Statement(s) received 13 April 2004 has been considered.

Please see the attached PTO-1449(s).

Specification

3.   The abstract of the disclosure (submitted 27 July 2004) is objected to because it is greater

than 150 words. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 112

4.   The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making
> and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it
> pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode
> contemplated by the inventor of carrying out his invention.

5.   Claims 1-23 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with

the written description requirement. The claim(s) contains subject matter which was not

described in the specification in such a way as to reasonably convey to one skilled in the relevant

art that the inventor(s), at the time the application was filed, had possession of the claimed

invention.

Applicant indicates that the bypass structure is within the data cache, however it is not

clear where this is taught in the specification. It is taught that the bypass structure is coupled to

the data cache, but not "within" the data cache (see originally filed claim 3).

All dependent claims are rejected as having the same deficiencies as the claims they

depend from.

Claim Rejections - 35 USC § 103

6.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

7.   Claims 1-6, 10, 12-13, and 22-23 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Dubey et al. (5,724,565) in view of Meier (6,523,109).

As per claim 1, 3, and 5, Dubey et al. teaches a central processing unit

("microprocessor") for processing multiple parallel instruction threads ("instruction streams").

The CPU includes a plurality of instruction buffers 141 (figure 1; "instruction queues") which

correspond to the multiple threads. See column 6, line 67, to column 7, line 2, and column 7,

lines 55-61. The CPU includes one or more functional units (see column 6, lines 24-26) and a

data cache (see column 6, line 49). Dubey et al. teaches different types of instructions, including

branch instructions ("first instructions", noting that Dubey et al. teaches that a branch unit is a type of functional unit; see column 1, lines 23-26 and 57-59), load instructions (column 28, line 23), and store instructions (column 28, lines 22-23). Dubey et al. also suggests a store queue ("bypass structure") and resolving memory dependencies between loads and stores. See column 28, lines 19-26.

Dubey et al. does not teach address matching logic and switching logic in association with the store queue ("bypass structure").

Meier teaches a store queue 68 (figures 3-4) for a data cache 44 (figure 1). The store queue includes a plurality of entries ("bypass structure...for receiving said store instructions...comprising multiple elements"). See figure 4. A comparison between a load address and entries in the store buffer is performed by a store queue number assignment circuit 60 ("address matching logic...for receiving load instructions..."). See column 10, lines 62-64, and column 11, lines 11-13 and 43-54. Meier teaches a merge/align circuit 120 in the data cache for merging bytes from the store queue with bytes from the data cache ("switching logic"). See column 18, lines 26-32. Meier also teaches that load (read) operation may match on multiple elements in the store queue ("wherein one of said read operations matches on multiple elements of said bypass structure", claim 3). See column 2, lines 20-23.

It would have been obvious to one of ordinary skill in the art to have modified the store queue of Dubey et al. to include the address matching and switching logic suggested by Meier (detailed above), because Meier teaches that such a store buffer implementation would conserve the amount of circuitry used and decreases average load latency (see column 1, lines 52-55 and 66-67), as well as optimizing code sequences (column 2, lines 27-32).

As per claims 2, 4, and 6, Meier teaches that the store buffer stores a quadword ("32 bits") of data per entry. See column 15, lines 35-36, and as shown in figure 4, there are more than 6 entries in the buffer ("comprising...six elements").

As per claim 10, Dubey et al. teaches that the data cache 170 is multi-ported (wherein "multi-port" may only be two ports). See column 9, lines 4-7.

As per claims 12 and 22, Meier teaches a multi-match condition where the youngest (i.e. "newest version") is selected from the store queue on a load (read) hit. See column 19, line 64, to column 20, line 9.

As per claims 13 and 23, Meier teaches a merge/align circuit 120 in the data cache for merging bytes from the store queue with bytes from the data cache. See column 18, lines 26-32.

8.   Claims 7-9, 11, 14-17, and 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dubey et al. in view of Meier in further view of Levy et al. (U.S. 2001/0004755).

As per claims 7, 14, and 18, it is noted that Dubey et al. has a number of instruction buffers that equals the number of threads that are executing simultaneously. See figure 1 and corresponding description. The combination of Dubey et al. and Meier et al. does not teach eight instruction buffers ("queues"), each corresponding to eight instruction threads ("streams"). Levy et al. teaches a processor executing a maximum of eight threads simultaneously. See page 7, paragraph [0085], line 7. It would have been obvious to one of ordinary skill in the art to have implemented 8 instruction buffer for 8 threads in the system of Dubey et al., as suggested by Levy et al., because Levy et al. teaches that with 8 threads stalling drops and provides the greatest choice of instructions to issue. See page 7, paragraph [0085], lines 7-10.

As per claims 8, 15, and 19, Dubey et al. teaches that the data cache 170 is multi-ported (wherein "multi-port" may only be two ports). See column 9, lines 4-7. If the cache memory only has two ports, then a maximum of two read (load) operations may be performed in on cycle on the data cache memory.

As per claims 9, 16, and 20, Dubey et al. teaches that the data cache 170 is multi-ported (wherein "multi-port" may only be two ports). See column 9, lines 4-7. If the cache memory only has two ports, then a maximum of two write (store) operations may be performed in on cycle on the data cache memory.

As per claims 11, 17, and 21, the combination of Dubey et al. and Meier does not teach that the threads are based on the MIPS instruction set architecture. Levy et al. teaches that it was know to utilize a MIPS instruction set processor in a multithreading system. See page 8, paragraph [0092]. It would have been obvious to have utilized a MIPS instruction set with the simultaneous multithreaded system of the combination of Dubey et al. and Meier because the MIPS architecture boosts programming performance by using an out-of-order instruction execution. See Levy et al, page 4, paragraph [0052].

Response to Arguments

9.   Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new ground(s) of rejection necessitated by Applicant's amendments to the claims.

Conclusion

10.   Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

All "OFFICIAL" patent application related correspondence transmitted by FAX must be directed to the central FAX number at **(703) 872-9306**:

"INFORMAL" or "DRAFT" FAX communications may be sent to the Examiner at **(703) 746-5693** (after October 14, 2004, the "INFORMAL" or "DRAFT" FAX number will be 571-273-4204), only after approval by the Examiner.
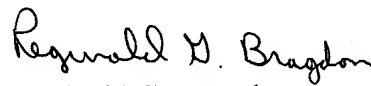
Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Fourth Floor (receptionist).

11.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reginald G. Bragdon whose telephone number is (703) 305-3823 (after October 14, 2004, the telephone number will be 571-272-4204). The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and every other Friday from 7:00 AM to 3:30 PM.

The examiner's supervisor, Mano Padmanabhan, can be reached at (703) 306-2903 (after October 14, 2004, the telephone number will be 571-272-4210).

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Reginald G. Bragdon
Primary Patent Examiner
Art Unit 2188

RGB
September 29, 2004